

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	39314	gate adj1 oxide\$1	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/13 16:48
2	BRS	L2	111	silicon adj1 nitride near5 (third near5 thickness,	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/13 16:48
3	BRS	L3	46	1 and 2	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/13 16:49
4	BRS	L4	44	3 and transistor	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/13 16:50
5	BRS	L5	131	(silicon adj1 nitride) near5 (third near5 silicon adj1 oxide	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/13 16:50

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	39	1 and 5	USPAT; US-PGP UB; EPO; JPO; 2002/04/03 DERWEN 17:17 T; IBM_TD B	
7	BRS	L7	70	(silicon adj1 nitride, near5 (third near5 silicon adj1 dioxide)	USPAT; US-PGP UB; EPO; JPO; 2002/04/03 DERWEN 17:31 T; IBM_TD B	
8	BRS	L8	41	and thickness	USPAT; US-PGP UB; EPO; JPO; 2002/04/03 DERWEN 17:18 T; IBM_TD B	
9	BRS	L9	40	8 and transistor	USPAT; US-PGP UB; EPO; JPO; 2002/04/03 DERWEN 17:18 T; IBM_TD B	
10	BRS	L10	134	(silicon adj1 nitride; near5 (third near5 dielectric)	USPAT; US-PGP UB; EPO; JPO; 2002/04/03 DERWEN 17:40 T; IBM_TD B	

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	111	10 and thickness	USPAT; US-PGP; UB; EPO; JPO; DERWEN; T; IBM_TD; B	2002/04/13 17:31
12	BRS	L12	11	11 and thickness	USPAT; US-PGP; UB; EPO; JPO; DERWEN; T; IBM_TD; B	2002/04/13 17:31
13	BRS	L13	262	(silicon adj1 nitride) near5 (third near5 insulating)	USPAT; US-PGP; UB; EPO; JPO; DERWEN; T; IBM_TD; B	2002/04/13 17:49
14	BRS	L14	113	13 and thickness	USPAT; US-PGP; UB; EPO; JPO; DERWEN; T; IBM_TD; B	2002/04/13 17:51
15	BRS	L15	4	15 and second adj1 thickness	USPAT; US-PGP; UB; EPO; JPO; DERWEN; T; IBM_TD; B	2002/04/13 17:52

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	117	6	15 and first adj1 thickness	USPAT; US-PGI UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/03 17:53
17	BRS	117	6	15 and first adj1 thickness	USPAT; US-PGI UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/03 17:53

	U	1	Document ID	Title	Current OR
	<input type="checkbox"/>	<input type="checkbox"/>	US 5384731 A	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	365/182
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5011040 B2	Semiconductor integrated circuit with an insulation structure having reduced permittivity	257/775
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6020644 A	Semiconductor memory device having bit lines and signal wiring layers different in thickness and process of fabricating thereof	257/775
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5449393 A	Semiconductor device and method of manufacturing the same	257/775
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5467308 A	Cross-point EEPROM memory array	257/775
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5384731 A	SRAM memory structure and manufacturing method thereof	365/182